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Attorney Docket No.: 00939s-050510US

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On JAN 16,2004 PRADEMIN

TOWNSEND and TOWNSEND and CREW LLP

By: Nicole M. Wartell

#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Michael J. Peters et al.

Application No.: 10/099,754

Filed: March 14, 2002

For: INTEGRATED CIRCUIT I/O PAD

CELL MODELING

Examiner: Not yet known

Art Unit: 3661

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37

CFR §1.97 and §1.98

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Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. This application is a continuation of and relies upon U.S. Patent Application No. 08/299,395 for an earlier effective filing date under 35 U.S.C. §120. In accordance with 37 CFR §1.98(d), copies of those references that have been previously submitted to or cited by the Office in the parent application are not enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

Michael J. Peters et al. Application No.: 10/099,754

Page 2

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that <u>no fee is required</u> for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

Chad E. King Reg. No. 44, 87

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, Eighth Floor San Francisco, California 94111-3834

3-571-4321

CEX:nmb

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(use as many sheets as necessary)

JAN 2,0 2004

Application Number 10/09

Filing Date March
First Named Inventor Peters
Art Unit 3661

Examiner Name Not we

Sheet

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of 2

	Complete if Known
Application Number	10/099,754
Filing Date	March 14, 2002
First Named Inventor	Peters, Michael J.
Art Unit	3661
Examiner Name	Not yet known
Attorney Docket Number	00939s-050510US

U.S. PATENT DOCUMENTS+							
	Document Number						
Cite No. ¹	Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			
A1	US-4488354	12-18-1984	Chan et al.				
A2	US-4683384	07-28-1987	Shibata et al.				
A3	US-4744084	05-10-1988	Beck et al.				
A4	US-4791357	12-13-1988	Hyduke				
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 A7	US-4980889	12-25-1990	DeGuise et al.				
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 A10	US-5317698	05-31-1994	Chan				
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 A12	US-5426591	06-20-1995	Ginetti et al.				
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 A14	US-5428750	06-27-1995	Hsieh et al.				
 A15	US-5452229	09-19-1995	Shankar et al.				
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ina	Cita	Fore	eign Patent Do	cument	Publication Date MM-DD-YYYY	Name of Patentee or	Pages, Columns, Lines, Where Relevant	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Application Number 10/099,754

Filing Date March 14, 2002

First Named Inventor Peters, Michael J.

Art Unit 3661

Examiner Name Not yet known

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Sheet 2 of 2 Attorney Docket Number 00939s-050510US

NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item						
Examiner Initials *	iner Cite (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue nun					
	C1	Agrawal, P. et al; "Can Logic Simulators Handle Bidirectionality and Charge Sharing?"; 1990 IEEE international Symposium on Circuits and Systems, May 1, 1990; pp. 411-414.				
	C2	Beresford, Roderic "An Emulator for CMOS ASICS"; VLSI Systems Design; May 4, 1987; pp. 8.				
	СЗ	Chranowska-Jeske, M. et al. "Improved I/O pad assignment for sea-of-gates placement algorithm", IEEE, Aug. 1992.				
	C4	Coelho; "A VHDL Standard Package for Logic Modeling"; IEEE Design & Test of Computers; vol. 7, No. 3, Jun. 1990; pp. 25-32.				
	C5	IBM Technical Disclosure Bulletin; Testing Multiple Discrete Software Components by Connecting Real and Simulated Hardware Components; pp. 1844,455, Vol. 30, No. 4; Sep., 1987.				
	C6	Nolan, Joe & Salt, Tom "The integration of power supply components within standard cell integrated circuits", IEEE, May 1989, p.13-5.1-5.4				

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1 °C/2		Application Number		10/099,754				
TRANSMITTAL			Filing Date		March 14, 2002			
<u> </u>	FORM			First Named Inventor		Peters, Michael J.		
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